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TOUCH SENSOR

GREENCHIP

GreenTouch5C[™] GTC08L **Capac**itive Touch Sensor

DATASHEET VER4.10



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${f 1}$. INTRODUCTION

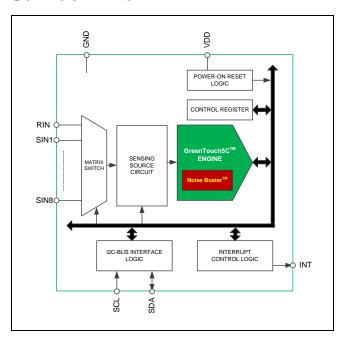
The GTC08L is one of the new GreenTouch5CTM capacitive touch sensor series. Especially the GTC08L can do capacitance sensing with 8 channels under above GreenTouch5CTM engine operation. Thanks to this epochal GreenTouch5CTM engine, the applications will be more robust and problem free against EMC, EMI, H/W variations, voltage disturbance, temperature drift, humidity drift and so on. *Especially, it doesn't make any issue against CS, RS, EFT, impulse and power ripple noise etc. environments occurred in any touch applications.*

The GTC08L can be applied under wide supply voltage range from 2.7V to 5.5V.

2. FEATURES

- 8 channels cap. Sensing input
- Simple & low cost solution
- Using minimum external component
- Embedded GreenTouch5C[™] Engine
 - Analog compensation circuit
 - Embedded digital noise filter
 - Intelligent sensitivity calibration
 - Embedded Noise Buster[™]
 (CS, RS, EFT, impulse and power ripple noise)
- Provide interrupt function
- Provide slide function
- Provide "REGISTER WRITING LOCK" function
- Wide supply voltage range: 2.7V to 5.5V
 - Single supply operation
- Package type
 - SOP-16L (9.90x3.90x1.40,e=1.27)
- RoHS compliant

3. BLOCK DIAGRAM



4. APPLICATIONS

- Multimedia Devices TV, DVD player, Blue ray player, Home theater system, Set top box and Etc.
- Home Appliance Refrigerator, Air cleaner, Air conditioner,
 Washing machine, Micro wave oven, Induction range, Cooker,
 Bidet, Water purifier, Humidifier, Wall switch and Etc.
- PC, OA and Others PC, LCD monitor, Fax, Copy machine, Lighting controls, Toys, Gaming devices and Etc.

5. ORDERING INFORMATION

Part No.	Package
GTC08L-SO	SOP-16L (9.90x3.90x1.40,e=1.27)

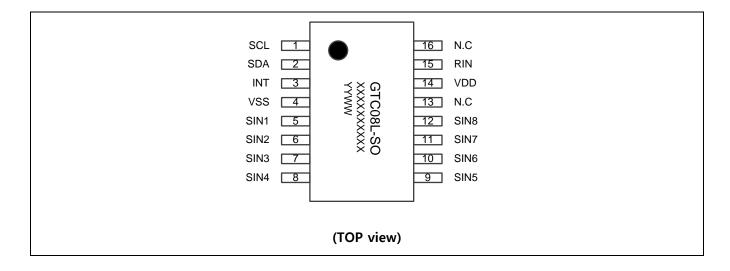
6. MARKING INFORMATION



7. PIN DESCRIPTION

This section describes the lists and illustrates the GTC08L of GreenTouch5CTM family pins as well as pin configuration. The GTC08L device is available in the following package.

7.1 PACKAGE INFORMATION (SOP-16L PACKAGE)



7.2 PIN CONFIGURATION

No.	Name	Туре	Description					
1	SCL	DI	I2C serial clock input					
2	SDA	DIO	I2C serial data communication pin					
3	INT DO		Interrupt output pin (Active LOW)					
4	GND	GND	Ground connection					
5	SIN1	AO	Channel 1: Touch sensing input					
6	SIN2	AO	Channel 2: Touch sensing input					
7	7 SIN3 AO		Channel 3: Touch sensing input					
8	SIN4 AO		Channel 4: Touch sensing input					
9	SIN5	AO	Channel 5: Touch sensing input					
10	SIN6	AO	Channel 6: Touch sensing input					
11	SIN7	AO	Channel 7: Touch sensing input					
12	SIN8	AO	Channel 8: Touch sensing input					
13	N.C							
14	VDD	PWR	Supply Voltage					
15	RIN	AO	Capacitance reference input					
16	N.C							

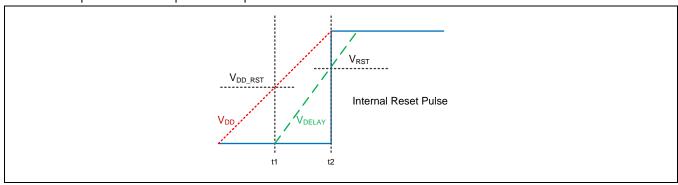
NOTE: DI: Digital Input, DO: Digital Output, DIO: Digital Input and Output, AI: Analog Input, AO: Analog Output, PWR: POWER

8. FUNCTION DESCRIPTION

8.1 INTERNAL RESET

The GTC08L has internal power reset function. The internal reset operation is used for initial power reset.

The internal power reset sequence is represented as below.



The internal V_{DELAY} voltage starts to rise when VDD come up to V_{DD_RST} level. The internal reset pulse is maintained as low between t1 and t2. During this low pulse period, the internal power reset operation is finished. Every time when VDD drops under V_{DD_RST} internal reset block makes V_{DELAY} signal low and then internal reset pulse drops to low. By above internal reset operation sequence GTC08L gets more certain and more correct power reset function than any others.

8.2 IMPLEMENTATION FOR TOUCH SENSING (SIN1~SIN8, RIN)

SIN inputs (SIN1~SIN8) and RIN input are used for touch detection of capacitance variation sensing. The SIN input pins are connected to touch sensing pad and catches capacitance variation caused by direct touch or approach. And RIN input for the reference capacitance is connected to a capacitor and resistor to compensate capacitance difference between SIN inputs and RIN input. The GTC08L compares each capacitance of SIN input and that of RIN input and determines touch detection of each channel when capacitance of each SIN input increases. So, for correct capacitance comparison between SIN inputs and RIN input, approximately equal initial-steady state capacitance between SIN inputs and RIN input are recommended. User can compensate initial-steady state capacitance difference between SIN inputs and RIN input by adding capacitor to RIN pin.

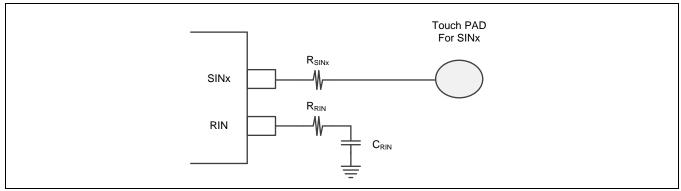
The GTC08L also has various intelligent sensing functions to determine valid touch from error or sensitivity problems caused by various environmental noise effects. These advanced sensing methods will help making faultless touch key systems under the worst conditions.

The internal intelligent sensitivity adjustment algorithm removes sensitivity rolling caused by system noise, circuit deviation, and circumstantial drift. The GTC08L has a special noise elimination filter for more powerful noise rejection and it will be very helpful for proper touch operation even if the system operates under deteriorative environment conditions.

The GTC08L SIN inputs have an internal series resistor for ESD protection. The additional external series resistors are profitable for prevention of abnormal actions caused by radiation noise or electrical surge pulse. In any case, if the additional external series resistor ($R_{SIN1\sim8}$, R_{RIN}) of each SIN and RIN input is required, then it should be less than 1.5K Ω to SIN and 10K Ω to RIN and the location of resister is recommended as closer to the SIN and RIN pins.

The SIN input routing lines are desirable to be routed as short as possible and the width of routing lines should be as narrow as possible and should be placed on bottom metal. In other words, a touch PAD and other parts should be placed on different metal each other. The additional extension line pattern of RIN input on application PCB can help prevention of abnormal actions caused by radiation noise, but excessive long RIN input line can be a reason for failure of touch detect. The SIN inputs and RIN input lines are desirable to be routed as far as possible from impedance varying path such as LED drive current path. All touch sensing pads are recommended to be surrounded by GND pattern in order to reduce noise influence.

Implementation circuit for SIN pins and RIN pin is shown in the following figure.

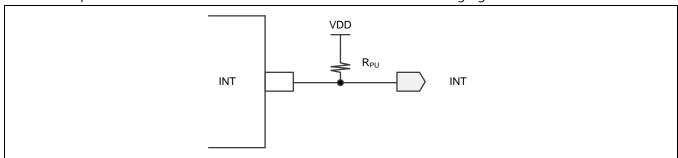


8.3 IMPLEMENTATION FOR INTERRUPT (INT)

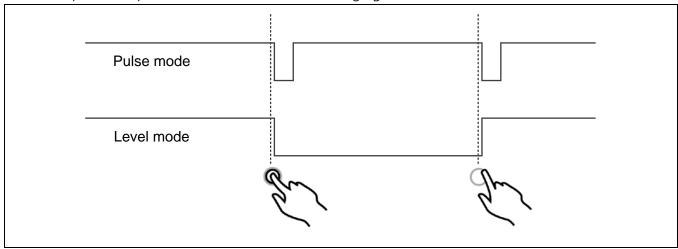
The GTC08L provides an interrupt (INT) function to reduce a communication load between MCU and GTC08L. The INT will indicate a point of time that the output status registers at the address 2Ah changes and MCU needs to read it. The INT pin has an open drain NMOS structure hence a couple of $k\Omega$ pull-up resistor must be required.

(See register address 10h = INT_MODE)

The basic implementations for active low modes are shown in the following figure.



Two interrupt mode operations are shown in the following figure.



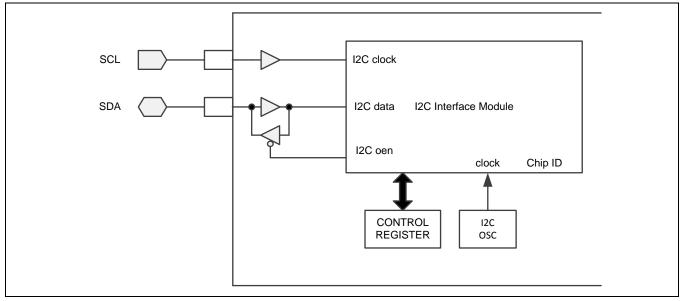
8.4 I2C INTERFACE (SCL, SDA)

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines; one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines be connected to a positive supply voltage via a internal pull-up resistor (typical $10k\Omega$) to prevent open gate leakage current in input mode. But the lines must be connected to a positive supply voltage via a pull-up additional external resistor.

The internal oscillator is disabled when all of both the SDA and SCL lines are high for saving current consumption.

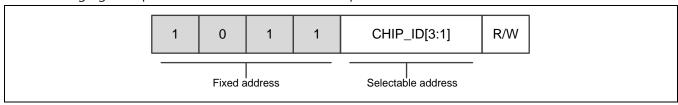
The simple internal block diagram for SCL and SDA is shown in the following figure.



8.4.1 DEVICE ADDRESSING

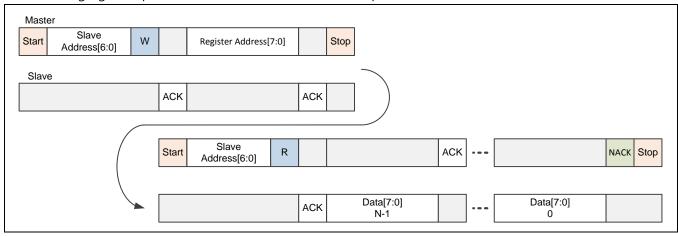
Following a START condition, the bus master must output the address of the slave it is accessing. The last bit of the slave address defines the operation to be performed. When set to logic 1, a read operation is selected, while a logic 0 selects a write operation.

The following figure represents the I2C slave address map.



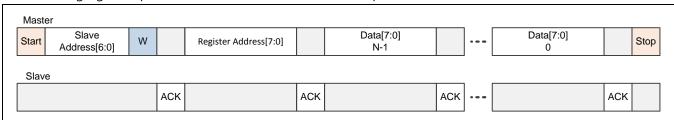
8.4.2 READ OPERATION

The following figure represents the I2C normal mode read operation.



8.4.3 WRITE OPERATION

The following figure represents the I2C normal mode write operation.



9. REGISTER DESCRIPTION

9.1 QUICK REGISTER MAP

0.11	D 04/	Reset				Da	nta				
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
00h											
01h	R/W	B8h	1	0	1	1	(CHIP_ID[3:1	.]	0	
02h											
03h											
04h	R/W	FFh	SIN8_ CH_EN	SIN7_ CH_EN	SIN6_ CH_EN	SIN5_ CH_EN	SIN4_ CH_EN	SIN3_ CH_EN	SIN2_ CH_EN	SIN1_ CH_EN	
05h											
06h											
07h											
08h											
09h											
0Ah	R/W	31h	0	0	1	1	0	0	0	MON_ RST	
0Bh	R/W	00h	0	0	0	0	0	0	0	SOFT_ RST	
0Ch	R/W	00h	0	0	0	0	0	0	0	I2C_ PU_DIS	
0Dh											
0Eh											
0Fh	R/W	5Ah		REGISTER_WRITE_LOCK							

NOTE: The blank register is assigned FFh data.

A al al	D //	Reset				Da	ita			
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	R/W	11h	0	0	0	INT_ MODE	0	0	0	MULTI_ MODE
11h	R/W	32h	0		EXP_TIME 0 0 EXP_I			EXP_EN	EXP_ MODE	
12h										
13h	R/W	0Ah	0	0	0	0		CAL_	TIME	
14h	R/W	00h	0	0	0	0	SEN_IDLE_TIME			
15h	R/W	05h	0	0	0	0	SEN_IDLE_TIME_SUFFIX			X
16h										
17h	R/W	04h	0	0	0	0	0 BUSY_TO_IDLE_TIME			TIME
18h	R/W	00h	0	0	0	0	0	0	0	I2B_ MODE
19h	R/W	00h	0	0	0	0	0	0	0	SLIDE _FUNC
1Ah										
1Bh										
1Ch										
1Dh										
1Eh										
1Fh										

NOTE: The blank register is assigned FFh data.

A d due se	D AM	Reset				Da	ita				
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
20h			0	0			SENSI	TIVITY1			
21h			0	0		SENSITIVITY2					
22h			0	0	SENSITIVITY3						
23h	D () A (OFL	0	0	SENSITIVITY4						
24h	R/W	0Fh	0	0			SENSI	TIVITY5			
25h			0	0		SENSITIVITY6					
26h			0	0	SENSITIVITY7						
27h			0	0	SENSITIVITY8						
28h											
29h											
2Ah	R	_	TOUCH_	TOUCH_	TOUCH_	TOUCH_	TOUCH_	TOUCH_	TOUCH_	TOUCH_	
ZAII	K	-	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	
2Bh	R	-	0	0	0	0	0	0	0	TOUCH_ OR	
2Ch										OK	
2Dh											
2Eh											
2Fh											

NOTE: The blank register is assigned FFh data.

9.2 REGISTER CONFIGURATION

9.2.1 01H REGISTER

Address	R/W	Reset	Data							
Address	IN/ VV	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
016	R/W B8h		1	0	1	1	(CHIP_ID[3:1	.]	0
01h		B8h	1	0	1	1	1	0	0	0

CHIP_ID[3:1]	Software selectable chip ID bit
	CHIP_ID[3:1] = changeable Chip ID bits

9.2.2 04H REGISTER

A al al	R/W	Reset								
Address	N/ VV	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	R/W		SIN8_	SIN7_	SIN6_	SIN5_	SIN4_	SIN3_	SIN2_	SIN1_
04h			CH_EN							
		FFh	1	1	1	1	1	1	1	1

SINn ⁽¹⁾ _CH_EN	Each of channel(SIN1~8) enable/disable bits
	0 = disable
	1 = enable
	NOTE: It's configured with the new offset when the SINn ⁽¹⁾ _CH_EN bit is enabled.

NOTE: (1) $n = SIN1 \sim SIN8 pin$

9.2.3 OAH REGISTER

A dalugas	D ///	Reset	Data								
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
	R/W			0	0	0	0	0	0	0	MON_
0Ah			U	U	U	U	U	U	U	RST	
		31h	0	0	1	1	0	0	0	1	

MON_RST	Internal and external reset monitoring bit 0 = not active and clear bit by user 1 = active and set bit by GTC08L
	NOTE: It's set '1' when GTC08L is reset.

9.2.4 OBH REGISTER

Address D.W.	D AM	Reset		Data								
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
					0		0	SOFT_				
0Bh	R/W		U	U	U	U	U	U	U	RST		
		00h	0	0	0	0	0	0	0	0		

SOFT_RST	Soft reset bit
	0 = Operation mode
	1 = Sleep mode.
	NOTE: Current consumption can be saved and Touch engine is not work in sleep mode.
	NOTE: It's configured with the new offset when the SOFT_RST bit is changed from sleep mode to operation mode.
	NOTE: All the value of register are not changed by SOFT_RST bit.

9.2.5 OCH REGISTER

Address R/W	D ///	Reset	Data								
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
				0	0	0	0	0	0	0	I2C_
0Ch	R/W		U	U	U	U	U	U	U	PU_DIS	
		00h	0	0	0	0	0	0	0	0	

I2C_PU_DIS	I2C pull-up control bit
	0 = I2C pull-up enable
	1 = I2C pull-up disable

9.2.6 OFH REGISTER

Address	D ///	Reset	eset Data							
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	D AAA				R	EGISTER_V	VRITE_LOC	K		
UFII	R/W	5Ah	0	1	0	1	1	0	1	0

REGISTER_WRITE_LOCK	Register write lock bit
	5Ah = All of registers can be read and write.
	Other = All of registers are locked. But it's possible to read registers.
	NOTE: When I2C is not used to write operation, it is recommended to prevent the write operation by using the "REGISTER_WRITE_LOCK" function.

9.2.7 10H REGISTER

Addross	ddress R/W	D ///	D /\/	D /\A/	D /\A/	D ///	D /\A/	R/W	D /\A/	D /\A/	D ///	D ///	Reset				Da	ıta			
Address		Value	Bit7	Bit6	Bit1	Bit0															
					0	0	0	INT_	0	0	0	MULTI_									
10h	R/W		U	U	U	MODE	U	U	U	MODE											
		11h	0	0	0	1	0	0	0	1											

INT_MODE	Interrupt operation mode selection bit
	0 = Pulse mode.
	1 = Level mode.
MULTI_MODE	Touch engine mode selection bit
	0 = Single touch mode
	1 = Multi touch mode.

9.2.8 11H REGISTER

Adduses	D ///	Reset	Data								
Address	Iress R/W	Value	Bit7	Bit6	Bit2	Bit1	Bit0				
				0 EXP_TIME				0	EXP_EN	EXP_	
11h	R/W		O		LVI TIIVIL		U	0	LXI _LIV	MODE	
		32h	0	0	1	1	0	0	1	0	

EXP_TIME ⁽¹⁾	Touch expire time selection bit								
	000 = 4sec	100 = 21sec							
	001 = 9sec	101 = 26sec							
	010 = 13sec	110 = 30sec							
	011 = 17sec	111 = 34sec							
EXP_EN	Touch expire enable bit								
	0 = disable								
	1 = enable								
	NOTE: It's configured with the new offset wh	en the touch expire function is executed.							
EXP_MODE	Touch expire mode bit								
	0 = expire count is not restarted wheneve	r a different touch occurs							
	1 = expire count is restarted if a different	touch occur							

NOTE: (1) Test condition: VDD = 5.0V, TA = $25^{\circ}C$

9.2.9 13H REGISTER

A d due s s	D ///	Rese	Reset	Data							
Address	s R/W Valu		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
126	D AM		0	0	0	0		CAL_	TIME		
13h	R/W	0Ah	0	0	0	0	1	0	1	0	

CAL_TIME ⁽¹⁾	Calibration time selection bit				
	0000 = 0msec + 1 period	1000 = 800msec + 1 period			
	0001 = 100msec + 1 period	1001 = 900msec + 1 period			
	0010 = 200msec + 1 period	1010 = 1000msec + 1 period			
	0011 = 300msec + 1 period	1011 = 1100msec + 1 period			
	0100 = 400msec + 1 period	1100 = 1200msec + 1 period			
	0101 = 500msec + 1 period	1101 = 1300msec + 1 period			
	0110 = 600msec + 1 period	1110 = 1400msec + 1 period			
	0111 = 700msec + 1 period	1111 = No Calibration			
	NOTE:				
	(1) The calibration time to protect from env	rironmental change			
	(2) Deviation: ±30% (@5.0V)				

NOTE: (1) Test condition: VDD = 5.0V, TA = $25^{\circ}C$

9.2.10 14H REGISTER

Address R/W	D ///	R/W Reset Value	Data								
	K/W		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
141 0004		0	0	0	0		SEN_IDI	_E_TIME			
14h	R/W	00h	0	0	0	0	0	0	0	0	

SEN_IDLE_TIME(1)	Idle time section bit								
	0000= 1msec	0100= 400msec	1000= 800msec	1100= 1200msec					
	0001= 100msec	0101= 500msec	1001= 900msec	1101= 1300msec					
	0010= 200msec	0110= 600msec	1010= 1000msec	1110= 1400msec					
	0011= 300msec	0111= 700msec	1011= 1100msec	1111= 1500msec					
	NOTE: The idle time	equation is as follows.							
	IDLE_TIME = SEN_IDLE_TIME[3:0] + SEN_IDLE_TIME_SUFFIX[3:0]								
	Ex> 110msec = 100ms	ec + 10msec							

NOTE: (1) Test condition: VDD = 5.0V, TA = $25^{\circ}C$

9.2.11 15H REGISTER

Address R/W	D AM	Reset	Data									
	K/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
1 F b	D /\A/		0	0	0	0	SEN_IDLE_TIME_SUFFIX					
15h R/W	R/W 05h	05h	0	0	0	0	0	1	0	1		

SEN_IDLE_TIME_SUFFIX(1)	Idle time suffix sec	ction bit							
	0000= 0msec	0100= 40msec	1000= 80msec	1100= 120msec					
	0001= 10msec	0101= 50msec	1001= 90msec	1101= 130msec					
	0010= 20msec	0110= 60msec	1010= 100msec	1110= 140msec					
	0011= 30msec	0111= 70msec	1011= 110msec	1111= 150msec					
		ne equation is as follo							
	IDLE_TIME = SEN_IDLE_TIME[3:0] + SEN_IDLE_TIME_SUFFIX[3:0]								
	Ex> 110msec = 100	msec + 10msec							

NOTE: (1) Test condition: VDD = 5.0V, TA = $25^{\circ}C$

9.2.12 17H REGISTER

Address R/W	Reset				Data					
	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
171-	D ///		0	0	0	0	0	BUSY	_TO_IDLE_T	IME
17h R,	R/W	04h	0	0	0	0	0	1	0	0

BUSY_TO_IDLE_TIME(1)	Busy to Idle time selection bit	
	000 = 0sec (disable)	100= 4sec
	001 = 1sec	101= 5sec
	010 = 2sec	110= 6sec
	011 = 3sec	111= 7sec

NOTE: (1) Test condition: VDD = 5.0V, TA = $25^{\circ}C$

9.2.13 18H REGISTER

A d duo sa	D ///	Reset	Data								
Address R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
18h R/W	R/W		0	0	0	0	0	0	0	I2B_ MODE	
	00h	0	0	0	0	0	0	0	0		

I2B_MODE	Idle to busy mode control bit
	0 = auto mode
	1 = manual mode

9.2.14 19H REGISTER

Address R	D //A/	Reset				Da	Data							
	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0				
19h	R/W		0	0	0	0	0	0	0	SLIDE _FUNC				
		00h	0	0	0	0	0	0	0	0				

SLIDE_FUNC	Slide function enable bit
	0 = disable
	1 = enable
	NOTE: After touch output, the IC operates in slide function within the time set in "BUSY_TO_IDLE_TIME" register at the address 17h.

9.2.15 20H~27H REGISTER

Address	R/W	Reset				Da	ıta			
Address	K/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			0	0			SENSIT	TVITY1		
			0	0			SENSIT	TVITY2		
			0	0	SENSITIVITY3					
20h			0	0	SENSITIVITY4					
~	R/W		0	0			SENSIT	TVITY5		
27h			0	0			SENSIT	TVITY6		
			0	0	SENSITIVITY7					
			0	0	SENSITIVITY8					
		0Fh	0	0	0	0	1	1	1	1

SENSITIVITYn(4)	Touch sensitivity control bit
	05h = Very high sensitive
	3Fh = Very high insensitive
	NOTE: It's recommended to use 0Ch~3Fh values at the sensitivity setting.

9.2.16 2AH, 2BH REGISTER

A al alva a a	D AM	Reset		Data						
Address	R/W	Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	D		TOUCH_							
ZAN	R	1	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
2Bh	R		0	0	0	0	0	0	0	TOUCH_
ZDII	K	-	0	U	U	U	U	0	U	OR

TOUCH_OUTn(1)	Each of SIN touch detection status bit
	0 = No touch detection
	1 = Touch detection.
	NOTE: It's set '1' when touch detection occur.
TOUCH_OR	Touch detection status bit
	0 = No touch detection
	1 = Touch detection.
	NOTE: It's set '1' when touch detection occur.

NOTE: (1) $n = SIN1 \sim SIN8 pin$

10. ELECTRICAL CHARACTERISTICS

10.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Тур.	Max	Units
Maximum supply voltage	V _{DD_MAX}		-0.3		6.0	V
Supply voltage range ⁽¹⁾	V_{DD_RNG}		-0.3		6.0	V
Voltage on any input pin	\/		-0.3		VDD	V
Voltage on any input pin	V _{IN_MAX}		-0.5		+0.3	V
Maximum current into any pin	I _{MIO}		-100		100	mA
Power dissipation	P _{MAX}		-		800	mW
Storage temperature	T _{STG}		-65		150	$^{\circ}$
Operating humidity	H _{OP}	8 hours	5		95	%
Operating temperature	T _{OPR}		-40		85	$^{\circ}$
Junction temperature	T _J		-40		125	°C

NOTE: (1) This is the real valid power supply voltage range considering allowable supply tolerance. It cannot be used as target supply voltage range which is separately presented at below I/O ELECTRICAL CHRACTERISTICS.

10.2 I/O ELECTRICAL CHARACTERISTICS

This section includes information about power supply requirements and I/O pin characteristics.

 $(TA = -25 \text{ to } 85^{\circ}\text{C}, V_{DD} = 2.7\text{V to } 5.5\text{V})$

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Target supply voltage	V _{DD}		2.7	3.0 / 5.0	5.5	V
Current consumption	I _{DD}	Standby mode	-	780	-	uA
		(VDD = 3.0V)				
		Standby mode	-	1000	-	uA
		(VDD = 5.0V)				
Input high voltage	V_{IH}	All input pins	0.7VDD	-	VDD	V
					+ 0.3	
Input low voltage	V_{IL}	All input pins	-0.3	-	0.3VDD	V
Output high voltage	V _{OH}	All output pins	VDD	-	-	V
		$(I_{OH} = -4mA,$	- 0.4			
		VDD = 5.0V)				
Output low voltage	V _{OL}	All output pins	-	-	0.4	V
		$(I_{OL} = 10 \text{mA},$				
		VDD = 5.0V)				
Output source current ⁽¹⁾	I _{SRC}	All output pins	-	-	-4	mA
		(Active high)				
Output sink current ⁽¹⁾	I _{SINK}	All output pins	-	-	10	mA
		(Active low)				
Output low leakage current	I _{LOL}		-	-	-1	uA
Output high leakage current	I _{LOH}		-	-	1	uA
SDA Internal Pull-up	R _{PU_SDA}		-	31	-	kΩ
Resister ⁽¹⁾						
SCL Internal Pull-up	R _{PU_SCL}		-	31	-	kΩ
Resister ⁽¹⁾						

NOTE:

(1) Test condition: VDD = 5.0V, $TA = 25^{\circ}C$ and normal operation mode under default control register value. (Unless otherwise noted)

10.3 RESET CHARACTERISTICS

 $(TA = -25 \text{ to } 85^{\circ}\text{C}, V_{DD} = 2.7\text{V to } 5.5\text{V})$

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
POR ⁽¹⁾ Time	t _{POR}		-	-	600	usec
POR voltage	V _{POR}		-	2.4	-	V

NOTE: (1) POR = Internal Power-On Reset

10.4 INTERRUPT OUTPUT CHARACTERISTICS

(TA = -25 to 85°C, V_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
INT low pulse width	t _{INT}		1	5	-	msec

10.5 SENSING INPUT CHARACTERISTICS

 $(TA = -25 \text{ to } 85^{\circ}\text{C}, V_{DD} = 2.7\text{V to } 5.5\text{V})$

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Minimum detectable input	ΔC _{S_MIN}		0.1	-	-	pF
capacitance variant						
Maximum input	C _{EXT_MAX}		-	-	100	pF
external capacitance						
Sensitivity selection steps	N _{SEN}		-	60	-	step
Sense OSC internal	R _{INT}		-	140	-	Ω
series resistor						

10.6 SYSTEM CHARACTERISTICS

(TA = -25 to 85°C, V_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Time for stable I2C	t _{I2C}		1	-	-	msec
communication after reset						
Time for stable Touch	t _{OP}		300	-	-	msec
Operating after Reset						
Touch On response time	t _{ON}	1 channel Touch at	-	80	-	msec
		all of register				
		default				

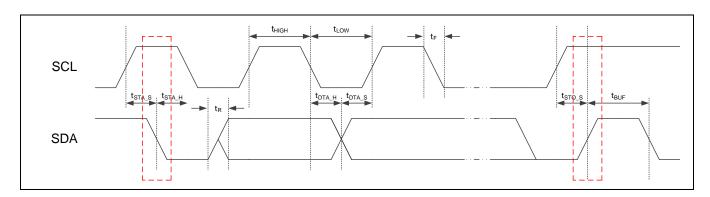
10.7 I2C INTERFACE TIMING CHARACTERISTICS

 $(TA = -25 \text{ to } 85^{\circ}\text{C}, V_{DD} = 2.7\text{V to } 5.5\text{V})$

Dawawatan	Comple el	Standar	d-mode	Fast-ı	mode	l lmia
Parameter	Symbol	Min.	Max.	Min.	Max.	Unit
SCL clock frequency	f _{SCL}	-	100	-	400	kHz
Hold time for START condition	t _{STA_H}	4.0	-	0.6	-	usec
LOW period of the SCL clock	t _{LOW}	4.7	-	1.3	1	usec
HIGH period of the SCL clock	t _{HIGH}	4.0	-	0.7	1	usec
Set-up time for START condition	t _{STA_S}	4.7	-	0.6	1	usec
Data hold time	t _{DAT_H}	5	-	40	1	nsec
Data set-up time	t _{DAT_S}	250	-	100	1	nsec
Rise time of both SDA and SCL	+		1000	20 +	300	ncoc
signals	t _R	-	1000	0.1 C _b ⁽²⁾	300	nsec
Fall time of both SDA and SCL	+		300	20 +	300	ncoc
signals	t _F	-	300	0.1 C _b ⁽²⁾	300	nsec
Set-up time for STOP condition	t _{STO_S}	4.0	-	0.6	-	usec
Bus free time between a STOP	+	4.7		1.3		ncoc
and START condition	t _{BUF}	4.7	-	1.5	-	usec
Capacitive load for each bus line	Cb	-	400		400	pF

NOTE:

- $(1) \ All \ values \ referred \ to \ VIH \ and \ VIL \ levels \ (please \ refer \ to \ I/O \ ELECTRICAL \ CHRACTERISTICS).$
- (2) C_b = total capacitance of one bus line in pF.



10.8 ESD CHARACTERISTICS

Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. During the device qualification, ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

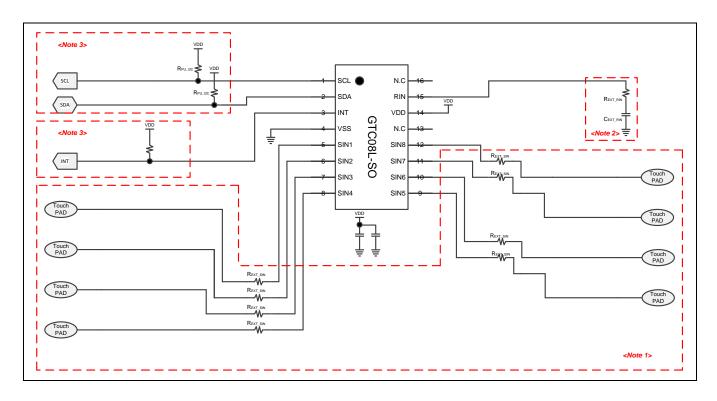
Test Mode	Symbol	Test Pin (Reference)	Max	Unit	Reference Document
		VSS, I/O (VDD)	±8000	V	
Human body model (HBM)	V _{HBM}	VDD, I/O (VSS)	±8000	V	JS-001-2014
		Every I/O (All I/O)	±8000	V	
		VSS, I/O (VDD)	±500	V	
Machine model (MM)	V _{MM}	VDD, I/O (VSS)	±500	V	JESD22-A115C :2010
		Every I/O (All I/O)	±500	V	
Charge device model (CDM)	V _{CDM}	Every Pin	±2000	V	JESD22-C101F :2013

10.9 LATCH-UP CHARACTERISTICS

Test Type	Symbol	Polarity	Max	Unit	Reference Document
Lacat	I _{LAT_POS}	Positive	200	mΑ	IECD 70E
I test	I _{LAT_NEG}	Negative	200	mA	JESD78E
V _{supply} over V _{DD_MAX}	V _{LAT_POS}	Positive	8.25	V	:2016

11. APPLICATION

11.1 EXAMPLE CIRCUIT (SOP-16L PACKAGE)



NOTE: $R_{EXT_RIN} = 560\Omega$ (recommend), $R_{EXT_SIN} = 560\Omega$ (recommend), $R_{PU_I2C} = 10K\Omega$ (recommend) $C_{EXT_RIN} = 3pF$ (recommend)

NOTE: The values of resistance and capacitance can be changed depending on the application set.

11.2 APPLICATION NOTES

Normally a touch sensing operation is ultimately impedance variation sensing. Hence a touch sensing system is recommended to be taken care of prevention of the external sensing disturbance. Although the GTC08L has enough noise rejection algorithms and various protection circuits to prevent error touch detection caused by noise and incapable sensing, it is better to take care in noisy applications such as home appliances. There are many measurable or invisible noises in system that can affect the impedance sensing signal or distort that signal. The main principal design issues and required attentions are such as below.

Power Line

- The touch sensor power line is recommended to be split from the other power lines such as relay circuits or LED power that can make pulsation noise on power lines.
- The big inductance that might exist in long power connection line can cause power fluctuation by other noise sources.
- The lower frequency periodic power noise such as a few Hz ~ kHz has more baneful influence on sensitivity calibration.
- An extra regulator for touch sensor is desirable for prevention above power line noises.
- The V_{DD} under shooting pulse less than internal reset voltage (V_{DD RST}) can cause system reset.
- The capacitor connected between V_{DD} and GND is somehow obligation element for buffering above power line noises. This capacitor must be placed as near to IC as possible.

• Sensing (Reference) Input Line for Touch Detect <Note1><Note2>

- The sensing lines for touch detection are desirable to be routed as short as possible and the width of routing path should be as narrow as possible.
- The sensing line for touch detection should be formed by bottom metal, in other words, an opposite metal of a touch PAD.
- The additional extension line pattern of RIN input on application PCB can help prevention of abnormal actions caused by radiation noise, but excessive long RIN input line can be a reason for failure of touch detect.
- The sensing line for touch detection is desirable to be routed as far as possible from impedance varying path such as LED drive current path.
- An unused sensing channel is desirable to be turned off by control register. (Recommendation)
- Additional external series resistors are profitable for prevention of abnormal actions caused by radiation noise or electrical surge pulse. The location of resister is better as near as possible to the

SIN and RIN pins for better stable operation.

(Refer to IMPLEMENTATION FOR TOUCH SENSING)

 All touch sensing pads are recommended to be surrounded by GND pattern to reduce noise influence.

I2C Interface and Interrupt Applications <Note3>

The SCL is I2C clock input pin and SDA is I2C data input/output pin. SCL and SDA have internal optional pull-up resistor. So, when I2C interface is not required, SCL and SDA pins can be floating. For high speed communication, SDA pin needs small pull-up resistor connected to V_{DD} to reduce pulse rising delay.

(Refer to I2C INTERFACE)

INT is for the output signal that indicates changing of sensing output data. This pin is output only pin
and has active low function. Because INT pin has open drain structure, pull-up resistor is required for
valid output.

(Refer to IMPLEMENTATION FOR INTERRUPT)

12. PACKAGE DIMENSION (SOP-16L PACKAGE)

